# Ultra High Density Flash Memory

## Abstract of the Disclosure

An ultra high density flash EEPROM provides increased nonvolatile storage capacity. A memory cell array includes densely packed memory cells, each cell having a semiconductor pillar providing shared source/drain regions for four vertical floating gate transistors that have individual floating and control gates distributed on the four sides of the pillar. Mutually orthogonal first gate lines and second gate lines provide addressing of the control gates. First source/drain terminals are row addressable by interconnection lines disposed substantially parallel to the first gate lines. Second source/drain terminals are column addressable by data lines disposed substantially parallel to the second gate lines. Both bulk semiconductor and silicon-on-insulator embodiments are provided. If a floating gate transistor is used to store a single bit of data, an area of only $F^2$ is needed per bit of data, where F is the minimum lithographic feature size. If multiple charge states (more than two) are used, an area of less than $F^2$ is needed per bit of data.